Alberto Parravicini – Curriculum Vitae – 2021

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Work Experience

Jan 2021 – Jul 2021 **Huawei European Research Center** – Zurich – Visiting Student Researcher
Researched HW/SW codesign for JIT compilers, *best-paper candidate at IISWC 2021*.

Feb 2018 – Apr 2020 **Oracle Labs** – Zurich & Milan – Research Assistant, Ph.D Student Collaborator
Created the first vertex embeddings-based Named Entity Disambiguation algorithm.
Developed a PoC translator from Natural Language to Graph Query Languages.
Researched GPU extensions for GraalVM. *2 patents pending*.

Jan 2018 – Jun 2018 **Unicredit** – Milan – Research & Development Intern
Developed a C library for entropy-based volatility proxies on high-frequency data.

Jul 2017 – Sep 2017 **AXA** – Brussels – Data Science Intern
Developed a deep-learning OCR pipeline to extract tabular data from insurance claims.

Education

2018 – Present Doctor of Philosophy in Computer Science and Engineering
at **Politecnico di Milano**.
Researching high-performance architectures for sparse linear algebra, graph analytics and recommender systems. Research lead of the GrCUDA project, in collaboration with Oracle Labs, managing a group of 10+ PhDs and students. Lecturer and TA of *Software Engineering* and *High-Performance Data & Graph Analytics*.

2015 – 2018 Master of Science Degree in Computer Science and Engineering
at **Politecnico di Milano**. Graduation Mark: **110/110, Cum Laude**

2017 **ATHENS:** Introduction to the Finite Elements Method, **TU Delft**, Netherlands

2016 **IDEA League Summer School:** Responsible Artificial Intelligence, **TU Delft**, Netherlands

2016 – 2017 Master of Science in Computer Science and Engineering
at **Ecole Polytechnique de Bruxelles**. (Exchange Student)

2012 – 2015 Bachelor of Science Degree in Engineering of Computing Systems
at **Politecnico di Milano**. Graduation Mark: **106/110**

Selected Publications

- **A. Parravicini**, L. G. Cellamare, M. Siracusa, M. D. Santambrogio, *Scaling up HBM Efficiency of Top-K SpMV for Approximate Embedding Similarity on FPGAs*, 2021 DAC.
- **A. Parravicini**, A. Delamare, M. Arnaboldi, M. D. Santambrogio, *A Runtime for Polyglot GPU Dynamic Scheduling with Resource-Sharing*, 2021 IPDPS.
- **A. Parravicini**, F. Sgherzi, M. D. Santambrogio, *A reduced-precision streaming SpMV architecture for Personalized PageRank on FPGA*, 2021 ASP-DAC. **Winner of the *XOHW 2020***, Ph.D. Category.
- **A. Parravicini**, R. Patra, D. B. Bartolini, M. D. Santambrogio, *Fast and Accurate Entity Linking via Graph Embedding*, 2019 GRADES-NDA.

Personal interests

- **Scientific interests** High-performance computing, graph analytics, sparse linear algebra, GPUs, FPGAs, computational finance
- **Other interests** Macro photography, hot enamel handicraft